PATENT

DECLARATION FOR UTILITY PATENT APPLICATION

AS A BELOW-NAMED INVENTOR, I HEREBY DECLARE THAT:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole/joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **LOGIC CIRCUIT PROTECTED AGAINST TRANSIENT DISTURBANCES**, the specification of which is attached hereto unless the following box is checked:

☒ was filed on as United States Application Serial No. 09/936,032 on 7 SEPTEMBER 2001

I HEREBY STATE THAT I HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE.

I acknowledge the duty to disclose information which is material to the patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Application No.	Country	Date of Filing (day/month/year)	Priority Claimed?	
PCT/FR00/00573	PCT	8 MARCH 2000	☒Yes	☐No
99/03027	FRANCE	9 MARCH 1999	☒Yes	☐No

I hereby claim benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Serial No.	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status
		☐Patented ☐Pending ☐Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

28-01-2002
Date

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Date

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Atty Docket: 514842000100 Serial No.: 09/936,032 Filed: September 7, 2001
Applicants: Michael NICOLAIDIS Mailing Date: February 4, 2002
Title: **LOGIC CIRCUIT PROTECTED AGAINST TRANSIENT DISTURBANCES**

Papers enclosed:

Transmittal (1 page)
Declaration (2 pages)

EJB1/vlc

RECEIVED BY THE U.S. PATENT AND TRADEMARK OFFICE

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